REMARKS

The present amendment is in response to the Office Action, dated October 23, 2002, where the Examiner has rejected claims 8, 9 and 13-22. By the present amendment and response, claims 8 and 9 have been amended to overcome the Examiner's rejections. Claims 15, 16, 20 and 21 have been amended to more clearly recite the present invention. Accordingly, claims 8, 9 and 13-22 are pending in the application. Reconsideration and allowance of pending claims 8, 9 and 13-22 in view of the following remarks are respectfully requested.

A. Rejection of Claims 8, 9, 13, 17, 18 and 22 under 35 U.S.C. §102(b)

The Examiner has rejected claims 8, 9, 13, 17, 18 and 22 under 35 USC §102(b) as being anticipated by **Van Dort et al.** (USPN 5,828,099) ("**Van Dort '099**"). Although Applicant respectfully disagrees with the Examiner's rejection, in order to expedite allowance of the present application, Applicant has amended claims 8 and 9 in response to the Examiner's rejection. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 8 and 9 and dependent claims 13, 17, 18 and 22, is patentably distinguishable over **Van Dort '099**.

Pending independent claims 8 and 9 are directed to a recessed tunnel oxide profile for improved reliability in NAND devices. As recited in amended independent claim 8, the device includes, "a gate insulating layer situated over said substrate, the gate insulating layer having a first thickness situated over said first region and said second region, and a second thickness situated over said third region, said first thickness being

greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform." Thus, the first thickness is greater than the second thickness. The first thickness is substantially uniform, i.e. the first thickness does not vary. Similarly, the second thickness is substantially uniform. The configuration of the gate insulating layer advantageously reduces the potential for oxide breakdown and/or current leakage in an overlap region, i.e. the first and second region recited in claim 8, while providing a suitable injection field for programming and erasing functions.

With regard to independent claim 8, **Van Dort '099** fails to disclose, teach or suggest the above recited limitations specified by claim 8. **Van Dort '099** discloses a nonvolatile memory cell comprising gate dielectric 10 having thickened portion 13 (Figure 1 and column 3 lines 36-40). Gate dielectric 10 comprises an oxide layer, wherein the oxide layer "becomes gradually thicker in the direction of the channel towards the source zone 4, which is favorable for the field distribution in the channel" (Figure 1 and column 3 lines 55-64). Thus, **Van Dort '099** teaches a device including a gate dielectric, analogous to the gate insulating layer of amended claim 8, having a non-uniform thickness. In contrast, amended claim 8 recites a gate insulating layer having a first thickness that is greater than a second thickness, wherein the first thickness and second thickness are substantially uniform. Therefore, the device of **Van Dort '099** does not reduce the potential for oxide breakdown and/or current leakage in an overlap region while providing a suitable injection field for programming and erasing functions.

Van Dort '099 cannot result in the present invention as recited in independent claim 8 because **Van Dort '099** fails to disclose or remotely suggest a device having a gate insulating layer having a first thickness that is greater than a second thickness, wherein the first thickness and second thickness are substantially uniform. Applicant believes the amendment to claim 8 further particularly points out and distinctly claims these limitations absent from cited references of record. Accordingly, applicant respectfully submits that rejection of amended claim 8 has been traversed, and that amended independent claim 8 and its corresponding dependent claims 13 and 17 should now be allowed.

The Examiner has rejected independent claim 9 for reasons similar to claim 8. Applicant has amended independent claim 9 to recite limitations similar to those recited in amended claim 8. In particular, claim 9 has been amended to recite, "a gate insulating layer situated over said substrate, the gate insulating layer having a first thickness situated over said first region and said second region, and a second thickness situated over said third region, said first thickness being greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform." Thus, applicant respectfully submits that independent claim 9, having been amended to recite language similar that in claim 8, and its corresponding dependent claims 18 and 22 should be allowed for at least the same reasons stated in conjunction with claim 8.

B. Rejection of Claims 14-16 and 19-21 under 35 U.S.C. § 103(a)

The Examiner has rejected claims 14-16 and 19-21 under 35 USC §103(a) as being unpatentable over **Van Dort '099**. Claims 14-16 and 19-21 depend from either amended claim 8 or amended claim 9. Thus, Applicant respectfully submits that claims 14-16 and 19-21 are patentable over **Van Dort '099** for the reasons discussed above in conjunction with claims 8 and 9. Accordingly, it is respectfully submitted that claims 14-16 and 19-21 should be allowed.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claims 8 and 9, and claims depending therefrom, is not suggested, disclosed, or taught by **Van Dort '099**. As such, amended independent claims 8 and 9 and dependent claims 13-22 are patentably distinguishable over **Van Dort '099**.

C. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 8 and 9, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 8, 9 and 13-22 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 8, 9 and 13-22 pending in the present application is respectfully requested.

Respectfully Submitted,
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Date: 1/22/03

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Version with Markings to Show Changes Made

In the Claims:

Claims 8, 9, 15, 16, 20 and 21 have been amended as follows:

8. (Twice Amended) A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type;

a gate insulating layer [formed] situated over said substrate, the gate insulating layer having a first thickness [formed] situated over said first region and said second region, and a second thickness [formed] situated over said third region, said first thickness being greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform; and

a control gate [formed on] situated over said gate insulating layer.

9. (Twice Amended) A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type; and

a gate insulating layer [formed] situated over said substrate, the gate insulating layer having a first thickness [formed] situated over said first region and said second

region, and a second thickness [formed] situated over said third region, said first thickness being greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform; and

an ONO stack [formed on] situated over said gate insulating layer.

15. (Amended) A memory cell as in claim 8, wherein [the electric] an injection field in [a region of overlap] an overlap region situated between said gate insulating layer and said first and second regions [is] ranges between [about] approximately 4 Mv/cm and approximately 6 Mv/cm.

16. (Amended) A memory cell as in claim 8, wherein [the electric] an injection field in [a region of overlap] an overlap region situated between said gate insulating layer and said third region [is] ranges between [about] approximately 8 Mv/cm and approximately 11 Mv/cm.

20. (Amended) A memory cell as in claim 9, wherein [the electric] an injection field in [a region of overlap] an overlap region situated between said gate insulating layer and said first and second regions [is] ranges between [about] approximately 4 Mv/cm and approximately 6 Mv/cm.

21. (Amended) A memory cell as in claim 9, wherein [the electric] an injection field in [a region of overlap] an overlap region situated between said gate insulating layer and said third region [is] ranges between [about] approximately 8 Mv/cm and approximately 11 Mv/cm.